

CLAIMS

I Claim:

Sub 12
 1. ~~On an integrated circuit, an interface block that provides an~~
 2 interface between an internal bus of the integrated circuit and a socket of a
 3 logic block, the interface block comprising:
 4 a synchronization module that performs any needed synchronization
 5 between a clock domain of the internal bus and a clock domain of the socket
 6 of the logic block;
 7 a translation module that, for data transferred between the internal
 8 bus and the socket of the logic block, provides translation of block encoding of
 9 the data;
 10 a queue module, that buffers data flowing between the internal bus
 11 and the socket of the logic block; and,
 12 a driver module that handles low level and electrical drive
 13 ~~specifications of the internal bus.~~

1 2. An interface block as in claim 1 wherein the synchronization
 2 module can be implemented as one of:
 3 a null synchronization block where no synchronization is required
 4 between the clock domain of the internal bus and the clock domain of the
 5 socket of the logic block;
 6 a ratio synchronization block where the clock domain of the internal
 7 bus is related to the clock domain of the socket of the logic block by a fixed
 8 multiplier ratio; and,

9 a full synchronization block where there is no phase relationship
10 between the clock domain of the internal bus and the clock domain of the
11 socket of the logic block.

1 3. An interface block as in claim 1 additionally comprising a plurality
2 of buffers used to pipeline the interface block, the plurality of buffers
3 including:

4 a first buffer between the synchronization module and the translation
5 module;

6 a second buffer between the translation module and the queue
7 module; and,

8 a third buffer between the queue module and the driver module.

1 4. A method for providing an interface between an internal bus of an
2 integrated circuit and a socket of a logic block within the integrated circuit,
3 the method comprising the steps of:

4 (a) performing any needed synchronization between a clock domain of
5 the internal bus and a clock domain of the socket of the logic block within a
6 synchronization module;

7 (b) providing any required translation of block encoding of data
8 transferred between the internal bus and the socket of the logic block using a
9 translation module;

10 (c) buffering data flowing between the internal bus and the socket of
11 the logic block using a queue module; and,

12 (d) handling low level and electrical drive specifications of the internal
13 bus using a driver module.

1 5. A method as in claim 4 wherein step (a) comprises the following
2 substeps:

3 (a.1) using a null synchronization block where no synchronization is
4 required between the clock domain of the internal bus and the clock domain
5 of the socket of the logic block;

6 (a.2) using a ratio synchronization block where the clock domain of
7 the internal bus is related to the clock domain of the socket of the logic block
8 by a fixed multiplier ratio; and,

9 (a.3) using a full synchronization block where there is no phase
10 relationship between the clock domain of the internal bus and the clock
11 domain of the socket of the logic block.

1 6. A method as in claim 4 additionally comprising the following step:
2 (e) providing buffers between modules to allow pipelined operation.

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3 ~~7. On an integrated circuit, an interface block that provides an~~
4 interface between an internal bus of the integrated circuit and a socket of a
5 logic block, the interface block comprising:

6 a plurality of modules connected in series, where any needed
7 synchronization between a clock domain of the internal bus and a clock
8 domain of the socket of the logic block, any required translation of block
9 encoding of data, any buffering of data flowing between the internal bus and

8 the socket of the logic block, and any low level and electrical drive
9 specifications of the internal bus are performed by the plurality of modules
10 ~~so that one module from the plurality of modules performs a single function.~~

1 8. An interface block as in claim 7 wherein a first module in the
2 plurality of modules is a synchronization module that performs any needed
3 synchronization between the clock domain of the internal bus and the clock
4 domain of the socket of the logic block.

1 9. An interface block as in claim 7 wherein one module in the
2 plurality of modules is a translation module that, for the data transferred
3 between the internal bus and the socket of the logic block, provides
4 translation of block encoding of the data.

1 10. An interface block as in claim 7 wherein one module in the
2 plurality of modules is a queue module, that buffers the data flowing
3 between the internal bus and the socket of the logic block.

1 11. An interface block as in claim 7 wherein one module in the
2 plurality of modules is a driver module that handles low level and electrical
3 drive specifications of the internal bus.

12. An interface block as in claim 7 additionally comprising a
plurality of buffers situated between modules in the plurality of modules, the
buffers used to pipeline the interface block.